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REMARKS

Claims 1-24 are under consideration in the application. Claims 23 and 24 stand allowed. Claims 1-6 and 12-22 stand rejected. Claims 7-11 have been objected to as being dependent upon a rejected base claim. Claim 4 is currently amended. No new matter is added. Reconsideration and further examination of the application is respectfully requested.

The invention relates to a method of conserving power in a computer by configuring the computer, based on a measured processor load, so that a lesser amount of speculative execution is enabled when the processor is lightly loaded than is enabled when the processor is heavily loaded.

Rejection of claim 4 under 35 U.S.C. § 112, second paragraph:

Claim 4 has been rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and claim the subject matter which Applicant regards as the invention. Specifically, the examiner asserts that the claim lacks antecedent basis for the limitation "than the first", occurring twice in the claim.

Claim 4 has been amended to clarify that in the first instance, "than the first" refers to the first value assigned to the processor load, and that in the second instance, "than the first" refers to the first measurement of the cache hit rate. Applicant believes the rejection to be overcome, and requests that it be withdrawn.

Rejection of claims 1, 13, 14, and 17 under 35 U.S.C. § 102(b):

Claims 1, 13, 14, and 17 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Buyuktosunoglu et al. (U.S. Pat. App. Pub. 2002/00530038) ("Buyuktosunoglu"). Applicant respectfully traverses the rejection. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 1 recites in part a method comprising measuring a processor load. The examiner cites paragraph [0025] of Buyuktosunoglu as disclosing this claim element. Applicant disagrees that the cited passage or any other part of Buyuktosunoglu

discloses measuring a processor load. Buyuktosunoglu's paragraph [0025] merely describes "counter-based hardware used ... to monitor [issue] queue activity", but does not suggest that "queue activity" relates in any way to processor load.

Elsewhere, the Buyuktosunoglu reference does describe "dynamically measuring an activity of the storage structure(s) and controlling the size of the storage structures(s) based on that measurement." (Buyuktosunoglu paragraph [0036]) Possible "computer architecture modules" that may be adjusted include an "out-of-order issue queue", "the main or a specific ... reorder buffer, branch prediction tables, cache and TLB ... memory structures." (Buyuktosunoglu paragraph [0020]) The structures are "sized down or up, depending on need or activity." (Buyuktosunoglu paragraph [0027]) Nowhere does Buyuktosunoglu suggest that any of these activity measurements is related to processor load.

Claim 1 further recites in part "configuring the computer, based on the processor load, so that a lesser amount of speculative execution is enabled when the processor is lightly loaded than is enabled when the processor is heavily loaded. Buyuktosunoglu does not expressly mention speculative execution, but does suggest resizing a "branch prediction table", which is a structure related to speculative execution. However, Buyuktosunoglu does not suggest that resizing the branch prediction table affects the amount of speculative execution that occurs. In fact, the method Buyuktosunoglu sizes its memory structures "depending on need or activity". (Buyuktosunoglu paragraph [0027]) In other words, Buyuktosunoglu configures its computer to accommodate the amount of an activity that is needed, not to affect the amount of the activity that occurs.

This difference is further highlighted by the fact that Buyuktosunoglu "preserves high processor performance". (Buyuktosunoglu paragraph [0021]) By contrast, Applicant's method may sacrifice performance when the performance is not needed. (Specification paragraphs [0022], [0023], [0028])

Clearly Buyuktosunoglu does not expressly describe each and every element of Applicant's claim 1. Neither does it describe them implicitly. In order to for a characteristic to be inherent in a reference, it is required that "...the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art." MPEP 2112 quoting *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). "The fact that a certain result or characteristic *may* occur or be present in the prior art is not sufficient to establish the inherency of that result or

characteristic." MPEP 2112 citing *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (emphasis in MPEP).

In the present case, the examiner has not shown that any of the activities measured by Buyuktosunoglu are necessarily related to processor load, nor has the examiner shown how changing the size of any of the structures listed by Buyuktosunoglu will necessarily affect the amount of speculative execution performed.

As is well known, different computer programs exercise processor resources differently. One of skill in the art may easily imagine a small, computationally-intensive program that contains few branch instructions, but that loads the processor heavily during execution. Such a program may be completely unaffected by a change in the size of even a branch prediction table. Even in a more complex program, the size of the branch prediction table would not necessarily affect the amount of speculative execution performed. The branch prediction table is a tool for improving the accuracy of choosing *which* code should be speculatively executed; it does not necessarily determine *whether* speculative execution is performed or not. (See Applicant's specification paragraphs [006] and [007].)

Clearly, Buyuktosunoglu does not disclose, expressly or inherently, each and every element of Applicant's claim 1, and therefore claim 1 is not anticipated by Buyuktosunoglu.

Claim 13 recites in part means for measuring a processor load. As is explained above with respect to claim 1, Buyuktosunoglu does not disclose this claim element.

Claim 13 further recites in part means for deciding, based on the processor load, whether to enable speculative execution. Nowhere does Buyuktosunoglu suggest enabling or disabling speculative execution. Changing the size of a branch prediction table, or even eliminating it, does not necessarily enable or disable speculative execution.

Clearly, Buyuktosunoglu does not disclose, expressly or inherently, each and every element of Applicant's claim 1, and therefore claim 1 is not anticipated by Buyuktosunoglu.

Claim 14 depends from claim 13 and adds further limitations, and is therefore also not anticipated by Buyuktosunoglu for at least this reason.

Claim 17 is not anticipated by Buyuktosunoglu for at least the reasons explained above with respect to claims 1 and 13.

Rejection of claims 2-6, 12, and 18-22 under 35 U.S.C. § 103(a):

Claims 2-6, 12, and 18-22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Buyuktosunoglu in view of Atkinson (U.S. Pat. No. 5,625,826). Applicant respectfully traverses the rejection because the examiner has not made out a prima facie case of obviousness.

"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." (MPEP 2143)

Without conceding either of the first two criteria, Applicant respectfully asserts that the combined references do not teach or suggest all of the limitations of the rejected claims.

Claims 2-6 and 12 depend from claim 1 and add further limitations. The examiner relies on Buyuktosunoglu to teach all of the elements of claim 1. As has been shown above, Buyuktosunoglu does not disclose all of the elements of claim 1. Atkinson does not cure this deficiency, and the examiner's prima facie case therefore fails.

Claims 18-22 depend from claim 17 and add further limitations. The examiner relies on Buyuktosunoglu to teach all of the elements of claim 17. As has been shown above, Buyuktosunoglu does not disclose all of the elements of claim 17. Atkinson does not cure this deficiency, and the examiner's prima facie case therefore fails.

Rejection of claims 15 and 16 under 35 U.S.C. § 103(a):

Claims 15 and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Buyuktosunoglu in view of Krimer et al. (U.S. Pat. App. Pub. 2004/0003215) ("Krimer"). Applicant respectfully traverses the rejection because the examiner has not made out a prima facie case of obviousness. The examiner's prima facie case is deficient for at least the reason that the combined references do not teach or suggest all of the limitations of the rejected claims.

Claims 15 and 16 depend from claim 13 and add further limitations. The examiner relies on Buyuktosunoglu to teach all of the elements of claim 13. As has been shown above, Buyuktosunoglu does not disclose all of the elements of claim 13. Krimer does not cure this deficiency, and the examiner's prima facie case therefore fails.

The examiner has made of record but not relied upon Davies et al. (U.S. Pat. No. 6,961,847). The cited references, even when combined, do not teach or suggest all of the elements of Applicant's claims.

Applicant believes this application is in condition for allowance, and such action is earnestly solicited.

Respectfully submitted,

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September 26, 2006
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